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# A 0.6 V Current Reference Based on the MOSFET Forward-Body-Biased ZTC Condition

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**Abstract**—This work presents a self biased current reference circuit based on the MOSFET Zero Temperature Coefficient (ZTC) condition. To achieve lower supply voltage ( $V_{DD}$ ) operation, the proposed circuit employs forward body biasing technique to decrease the MOSFET ZTC biasing point. In addition, a body-driven pseudo differential Operational Transconductance Amplifier (OTA) is used to further reduce the minimum supply voltage. From transistor-level simulations, the current reference is predicted to have an Effective Temperature Coefficient ( $TC_{eff}$ ) of 65 ppm/ $^{\circ}C$  from  $-55$  to  $125$   $^{\circ}C$  and a fabrication sensitivity of  $\sigma/\mu = 6.5$  %, including process and mismatch variability. The power supply sensitivity is around 0.75 %/V for this new reference.

## I. INTRODUCTION

Being an essential building block for analog designs, current references work as a biasing reference for many other circuits. To suit the recent nanoscale CMOS technology low voltage supply ( $V_{DD}$ ) constraints [1] and/or the requirements of low power applications [2]–[4], several current references have been proposed [5]–[8]. Among them, it can readily be seen that the usage of the MOSFET Zero Temperature Coefficient (ZTC) condition has been showing itself as good approach mainly due to its programability [9]–[12] and its availability in advanced MOSFETs technologies, such as UTBB SOI and FinFET devices [13].

As a new alternative, this work presents a novel ZTC based current reference circuit which uses forward body biasing technique to decrease the MOSFET ZTC bias point. In addition, to further improve the circuit performance in low  $V_{DD}$  operation, a bulk-driven Operational Transconductance Amplifier (OTA) [14], [15] within proposed current reference is used.

The paper has the following structure. In Section II, the forward body biasing technique applied in the ZTC operating point is described. In Section III, the self-biased CMOS current reference is analysed and designed. The transistor level simulation results are presented in section IV, followed by comparisons to other references proposed in the literature. Finally, in section V, the concluding remarks are drawn.

## II. MOSFET FORWARD-BODY-BIASED ZTC CONDITION

The ZTC condition comes from the mutual cancellation of the mobility and threshold voltage dependencies on temperature [5]. Fig. 1 shows the drain current w.r.t. the gate-source voltage ( $V_{GS}$ ) of a saturated long-channel  $10 \mu m$  width by  $10 \mu m$  length 180nm process NMOS transistor, simulated

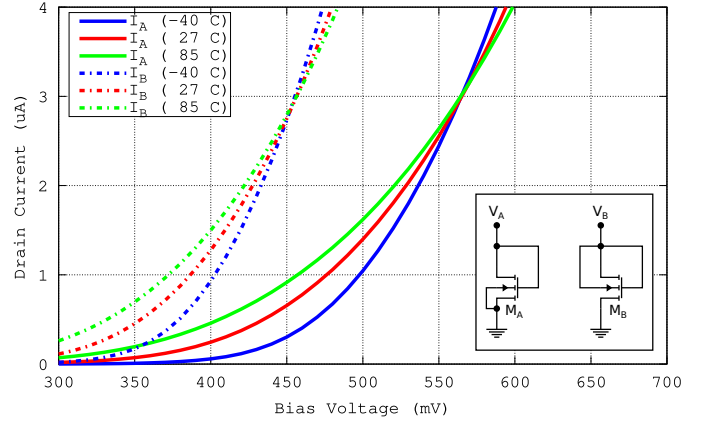


Fig. 1: NMOSFET ZTC condition in diode configuration: (a) Gate connected and (b) Forward-Body-Biased connected

under  $-40^{\circ}C$ ,  $27^{\circ}C$  and  $85^{\circ}C$  temperatures, for both the gate and forward-body-biased diode-connected configurations. The ZTC operation points can be seen around  $V_{GB} \approx 570mV$  and  $V_{GB} \approx 450mV$  for the gate and forward-body-biased diode-connected configurations, respectively. In these bias points, the currents are tolerant to temperature variation.

In [5], MOSFET ZTC and its vicinity conditions have been modeled and expressed by (1) and (2). Which explain the lower voltages for the ZTC behavior in the the forward-body-biased configuration (negative  $V_{SB}$ ).

$$V_{GS}(T) \approx V_{GZ} - \frac{\alpha_{V_{T0}} \Delta i_f}{2i_{fz}} T \quad (1)$$

where

$$V_{GZ} = V_{T0}(T_0) + (n-1)V_{SB} - \alpha_{V_{T0}} T_0 \quad (2)$$

$V_{GS}$  is the gate-source voltage,  $V_{GZ}$  is the ZTC gate-source voltage,  $\beta_z$  is the ZTC slope,  $\Delta i_f$  indicates how far the transistor is biased from the ZTC operating point,  $i_f$  is the forward inversion level,  $i_{fz}$  is the ZTC forward inversion level,  $T$  is the temperature,  $V_{T0}(T_0)$  is the threshold voltage at room temperature,  $n$  is the slope factor,  $V_{SB}$  is the source-bulk voltage and  $\alpha_{V_{T0}}$  is the thermal coefficient of the threshold voltage.

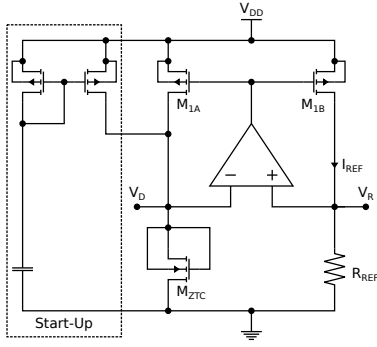


Fig. 2: Self-biased CMOS current reference concept based on the forward-body-biased ZTC operation condition [5].

### III. PROPOSED SELF BIASED CURRENT REFERENCE

Figure 2 shows a self-biased current reference based on the MOSFET ZTC operation condition, as presented in [5]. The MOSFET device  $M_{ZTC}$ , while in diode configuration (in this case, forward-body-biased connected), if biased properly with a specific  $V_{GS}$  gate-source voltage, outputs a drain current tolerant to temperature variations. The main idea of this current reference topology is to use ZTC vicinity of a MOSFET transistor to compensate the thermal drift of a polysilicon reference resistor  $R_{REF}$ , resulting on an equilibrium bias point with small temperature dependence. The Eqs. (3) and (4) describe how to size  $R_{REF}$  and  $M_{ZTC}$  aspect ratio properly [5].

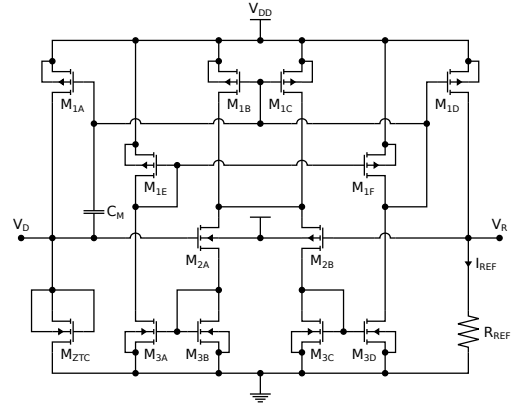
$$R_{REF} \approx \frac{V_{GZ}}{I_{REF}(1 - \alpha_1 T_0)} = \frac{V_{T0}(T_0) + (n - 1)V_{SB} - \alpha_{V_{T0}} T_0}{I_{REF}(1 - \alpha_1 T_0)} \quad (3)$$

$$(W/L)_{ZTC} = \frac{2n \left( \frac{-2\alpha_1 R_{REF}}{\alpha_{V_{T0}}} + \frac{1}{I_{REF}} \right)^{-1}}{\mu_n(T_0) T_0^2 C'_{ox} \alpha_{V_{T0}}^2} \quad (4)$$

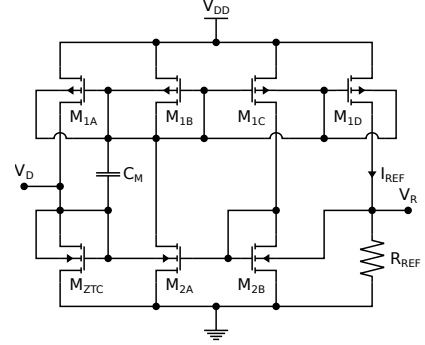
where  $\alpha_1$  is poly resistor thermal dependence,  $C'_{ox}$  is the gate capacitance per unit of area and  $I_{REF}$  is the output reference current.

The minimum supply voltage required by this topology is limited either by the  $M_{ZTC}$  biasing voltage or by the OTA. Figure 3a shows a version of the previous circuit using conventional OTA. This OTA is composed of three stacked transistors which must be in the saturation region in order the circuit functions properly.

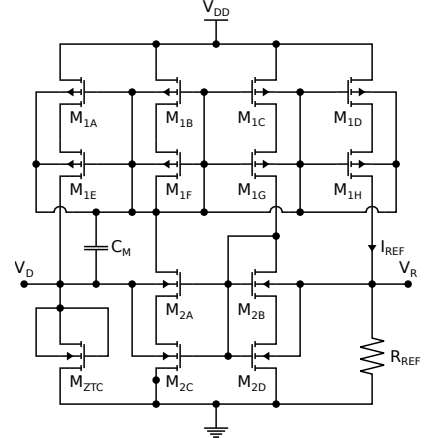
The circuit shown in Figure 3b uses a body input OTA, which is composed by two stacked transistors and can possibly function with a lower supply voltage. However, the use of the body terminal as input has its drawbacks. The forward biased body-source junction works as a forward biased diode and draws current from the input source. More importantly, the input impedance varies greatly with temperature, which can interfere in the reference transistor  $M_{ZTC}$  biasing point. As the reference transistor  $M_{ZTC}$  gate and body terminals



(a) Gate input OTA version



(b) Body input OTA version



(c) Body input OTA enhanced version

Fig. 3: Current reference circuits with OTA variations

are shorted in order to lower its ZTC biasing point,  $V_D$  is then lowered and the current drawn by the differential pair parasitic diode is decreased, as can be seen in Fig. 1. The same technique is used in the current mirror composed of the transistors  $M_{1A-D}$  to decrease their inversion levels and, consequently, their saturation voltages.

Also, the body-drain small signal transconductance  $g_{mb}$  is a fraction of the gate-drain transconductance  $g_{mg}$  so that the OTA has a reduced voltage gain compared to the conventional gate input OTAs. To mitigate this, the transistors  $M_{1A-D}$  and  $M_{2A-B}$  are replaced by composite transistors [16], which can

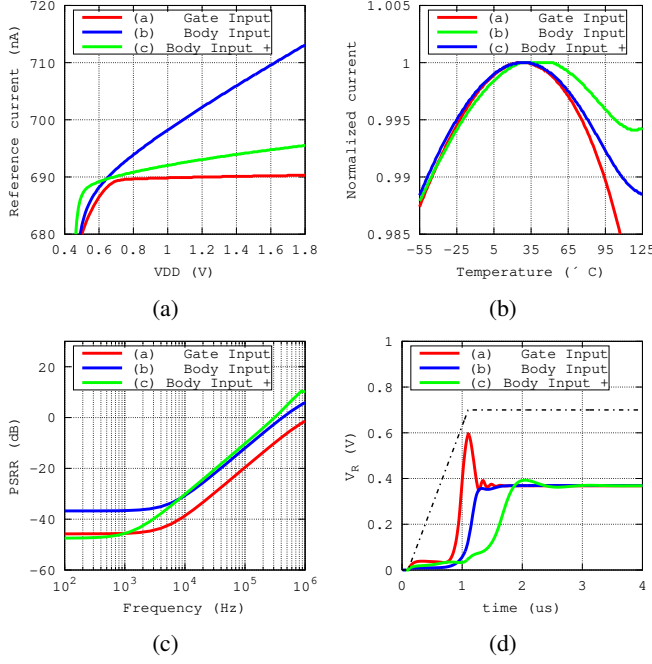


Fig. 4: Current reference comparison: (a) Output current reference power supply sensitivity, (b) Normalized current reference temperature sensitivity, (c) Power Supply Rejection and (d) Start-Up Time

be made equivalent to single transistors with larger output impedance.

#### IV. SIMULATION RESULTS

To validate the proposed current reference, three versions have been designed using the same forward-biased ZTC transistor and polyresistor with the Silterra IoT 0.18  $\mu\text{m}$  PDK. All simulation results herein presented are at transistor level using Cadence Virtuoso<sup>TM</sup> software and BSIM4.5 MOSFET models. The three versions differ only by the OTA, as shown in Figure 3, and the transistor sizes are shown in Table I.

	$k \times m \times W/L$
Gate Input OTA	
$M_{1A-F}$	$16 \times 4 \times 700 \text{ nm} / 360 \text{ nm}$
$M_{2A-B}$	$16 \times 4 \times 700 \text{ nm} / 360 \text{ nm}$
$M_{3A-D}$	$16 \times 4 \times 700 \text{ nm} / 360 \text{ nm}$
Body Input OTA	
$M_{1A-D}$	$16 \times 1 \times 700 \text{ nm} / 2.82 \mu\text{m}$
$M_{1A-B}$	$16 \times 1 \times 700 \text{ nm} / 2.82 \mu\text{m}$
Enhanced Body Input OTA	
$M_{1A-D}$	$16 \times 1 \times 700 \text{ nm} / 2.82 \mu\text{m}$
$M_{1E-H}$	$16 \times 4 \times 700 \text{ nm} / 360 \text{ nm}$
$M_{1A-B}$	$16 \times 4 \times 700 \text{ nm} / 360 \text{ nm}$
$M_{1C-D}$	$16 \times 1 \times 700 \text{ nm} / 2.82 \mu\text{m}$
$M_{ZTC}$	$1 \times 1 \times 10.0 \mu\text{m} / 10.0 \mu\text{m}$
$R_{REF}$ (535 k $\Omega$ )	$24 \times 450 \text{ nm} / 7.75 \mu\text{m}$
$C_M$ (1 pF)	$1 \times 20 \mu\text{m} / 50 \mu\text{m}$

TABLE I: Transistor dimensions

Figure 4 shows how each circuit version compares to each other in several performance aspects. Figure 4a shows the

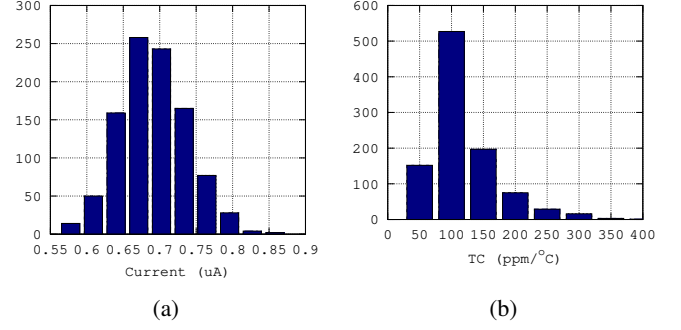


Fig. 5: Monte Carlo simulation including process and mismatch: (a) Output current reference mismatch and (b) Temperature coefficient mismatch

reference current  $I_{REF}$  versus power supply. All circuits were designed at the same biasing point and output a 690 nA reference current, but they differ at the power supply sensitivity and minimum operational supply voltage. The gate input OTA, body input OTA and enhanced body input OTA versions have a minimum operational voltage of approximately 0.7 V, 0.6 V and 0.6 V, and 0.02 %/V, 3.00 %/V and 0.75 %/V supply voltage sensitivity respectively.

Figure 4b depicts  $I_{REF}$  temperature sensitivity. The gate input OTA has Effective Temperature Coefficient ( $TC_{eff}$ ) of approximately 80 ppm/ $^{\circ}\text{C}$ , over a temperature range from -40 to 85 $^{\circ}\text{C}$ . On the other hand, the body input OTA versions have an  $TC_{eff}$  of approximately 65 ppm/ $^{\circ}\text{C}$  over the temperature range from -55 to 125 $^{\circ}\text{C}$ . It is worthwhile to mention that the body input versions were optimized for temperature range and the same biasing point was used for the gate bias version so that they would output the same reference at typical conditions.

Figure 4c depicts  $I_{REF}$  power supply rejection ratio of each circuit version at a 700 mV supply voltage operation. As can be noticed, the enhanced body input OTA version exhibits a better DC PSRR than simple bulk input OTA version, but they exhibit almost the same behavior at higher frequencies. The gate OTA version has a similar DC PSRR at this supply voltage operation point, yet it has a better performance at higher frequencies, due to transistor gate-drain transconductances being considerably higher than body transconductances.

Figure 4d shows a transient simulation depicting the start-up time and circuit stability with a 1  $\mu\text{s}$  rise time 700 mV supply voltage pulse signal. All circuits use a compensation capacitor  $C_M$  to ensure stability, but only the OTA version needs a start-up circuit, as shown in Figure 2.

Figure 5 shows the enhanced body input current reference version  $I_{REF}$  and  $TC_{eff}$  spread from 1000 monte carlo runs, including process variation and mismatch. Fig. 5a shows the reference current spread with a  $\sigma/\mu = 6.5\%$ . While Fig. 5b presents a  $TC_{eff}$  spread with 99 % of samples below the 300 ppm/ $^{\circ}\text{C}$ . In order to correct the process variability undesired effects, a calibration scheme, such as digitally trimmed reference resistors [18] could be used.

Table II presents a summary of our topologies and com-

	This Work**			[5]**	[6]*	[7]**	[17]*
	(a)	(b)	(c)				
Technology	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Temperature range (°C)	-55 to 100	-55 to 125	-55 to 125	-40 to 85	-70 to 100	-25 to 125	0 to 100
Minimum Power Supply (V)	0.7	0.6	0.6	1.4	1.0	0.65	1.0
$I_{REF}$ ( $\mu A$ )	0.690	0.690	0.690	5.0	0.042	0.01	144
Total current ( $\mu A$ )	4.14	2.76	2.76	196	-	0.09	-
Power ( $\mu W$ )	2.90	1.65	1.65	342	-	0.07	227
Power Supply Sensitivity (%/V)	0.02	3.00	0.75	2.5	0.2	0.01	-
Temperature coefficient (ppm/°C)	80	65	65	15	3000	350	185
PSRR (dB)	45.8	36.8	48.5	-	-	-	-
Start-Up Time ( $\mu s$ )	2.0	2.0	3.0	-	-	5500	-
Area $mm^2$	-	-	0.008	0.010	0.010	0.025	-

TABLE II: Comparison of CMOS current references

\* Measured results \*\* Simulated results

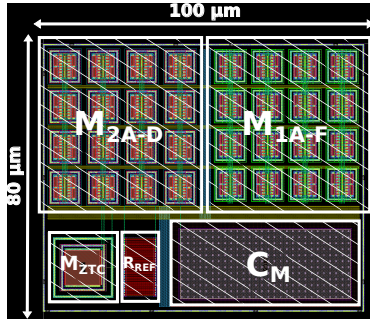


Fig. 6: Enhanced Bulk Driven OTA version self biased current reference layout

parison of published current references in similar process technologies. The main advantage of the presented solution is its low supply voltage requirement.

## V. CONCLUSION

Forward body biasing lowers the MOSFET ZTC condition and this technique can be used to decrease the minimum supply voltage, as it has been demonstrated in the proposed self-biased current reference. A body input OTA has also been used to further reduce the minimum supply voltage and composite transistors were implemented to improve the OTA voltage gain. Transistor-level simulation results have shown  $TC_{eff}$  of 65 ppm/°C from -55 to 125 °C and a fabrication sensitivity of  $\sigma/\mu = 6.5\%$ , with 0.75 %/V of power supply sensitivity.

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## REFERENCES

- [1] R. H. Dennard, "Past Progress and Future Challenges in LSI Technology: From DRAM and Scaling to Ultra-Low-Power CMOS," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 29–38, Spring 2015.
- [2] O. Aiello, P. Crovetto, and M. Alioto, "Standard Cell-Based Ultra-Compact DACs in 40-nm CMOS," *IEEE Access*, vol. 7, 2019.
- [3] N. Pinckney, D. Blaauw, and D. Sylvester, "Low-Power Near-Threshold Design: Techniques to Improve Energy Efficiency," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 49–57, Spring 2015.

- [4] O. Aiello, P. S. Crovetto, and M. Alioto, "Fully synthesizable low-area digital-to-analog converter with graceful degradation and dynamic power-resolution scaling," *IEEE Tran. on Circuits and Syst. I: Reg. Papers*, vol. 66, no. 8, pp. 2865–2875, Aug 2019.
- [5] P. Toledo, H. Klimach, D. Cordova, S. Bampi, and E. Fabris, "MOSFET ZTC Condition Analysis for a Self-biased Current Reference Design," *Journal of Integrated Circuits and Systems*, vol. 10, no. 2, pp. 103–112, 2015.
- [6] E. M. Camacho-Galeano, J. Q. Moreira, M. D. Pereira, A. J. Cardoso, C. Galup-Montoro, and M. C. Schneider, "Temperature performance of sub-1V ultra-low power current sources," in *2008 IEEE International Symposium on Circuits and Systems*. IEEE, 2008, pp. 2230–2233.
- [7] A. Far, "Current reference for energy harvesting: 50um per side, at 70 nW, regulating to 125c," in *2014 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC)*. IEEE, 2014, pp. 1–5.
- [8] D. Cordova, A. C. de Oliveira, P. Toledo, H. Klimach, S. Bampi, and E. Fabris, "A sub-1V, nanowatt, ZTC based zero-VT temperature-compensated current reference," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017, pp. 1–4.
- [9] P. Toledo, D. Cordova, H. Klimach, S. Bampi, and P. S. Crovetto, "A 0.31.2V Schottky-Based CMOS ZTC Voltage Reference," *IEEE Tran. on Circuits and Syst. II: Express Briefs*, vol. 66, no. 10, pp. 1663–1667, Oct 2019.
- [10] D. Cordova, P. Toledo, H. Klimach, S. Bampi, and E. Fabris, "A High-PSR EMI-Resistant NMOS-Only Voltage Reference Using Zero- $V_T$  Active loads," *IEEE Transactions on Electromagnetic Compatibility*, vol. 59, no. 4, pp. 1347–1355, Aug 2017.
- [11] P. Toledo, H. Klimach, D. Cordova, S. Bampi, and E. Fabris, "Resistor-less switched-capacitor current reference based on the MOSFET ZTC condition," in *2015 IEEE 6th Latin American Symposium on Circuits Systems (LASCAS)*, Feb 2015, pp. 1–4.
- [12] —, "Self-biased CMOS current reference based on the ZTC operation condition," in *2014 27th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Sep. 2014, pp. 1–7.
- [13] J. Martino, V. Mesquita, C. Macambira, V. Itocazu, L. Almeida, P. Agopian, E. Simoen, and C. Claeys, "Zero temperature coefficient behavior for advanced mosfets," in *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct 2016, pp. 785–788.
- [14] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process," *IEEE Tran. Circuits Syst. I: Reg. Papers*, vol. 61, no. 6, pp. 1609–1617, June 2014.
- [15] O. Abdelfattah, G. W. Roberts, I. Shih, and Y. Shih, "An Ultra-Low-Voltage CMOS Process-Insensitive Self-Biased OTA with Rail-to-Rail Input Range," *IEEE Tran. Circuits Syst. I: Reg. Papers*, vol. 62, no. 10, pp. 2380–2390, Oct 2015.
- [16] C. Galup-Montoro, M. C. Schneider, and I. J. Loss, "Series-Parallel Association of FET's for High Gain and High Frequency Applications," *IEEE J. of Solid-State Circuits*, vol. 29, no. 9, pp. 1094–1101, 1994.
- [17] A. Bendali and Y. Audet, "A 1-V CMOS Current Reference with Temperature and Process Compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 7, pp. 1424–1429, 2007.
- [18] M. Heinrich, J. Heidrich, T. Ussmueller, and R. Weigel, "Concept for electronic calibration of a CMOS voltage reference," in *2010 IEEE International Conference on Wireless Information Technology and Systems*. IEEE, pp. 1–4.